David Le Chan

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Education

Carnegie Mellon University (CMU) | Pittsburgh, PA

Masters of Science in Electrical and Computer Engineering — Expected May 2027

- GPA: 4.0/4.0

Bachelors of Science in Electrical and Computer Engineering with University Honors — Graduated May 2026

- GPA: 3.8/4.0; *Senior Leadership Recognition Award, 6x Dean's List Recipient*

Work Experience

Hardware Development Engineering Intern — May 2026 - August 2026

Annapurna Labs (Amazon AWS), Machine Learning Acceleration | Austin, TX

- Verified and deployed PCIe Gen5/Gen6 connectivity to scale machine learning acceleration systems
- Authored and executed qualification tests for switches, expanding high-speed rack-level test coverage
- Migrated tests to a Lua orchestration framework to enable continuous validation via AWS test infrastructure
- Identified mechanical defects impacting 100k+ units, driving resolution to meet deployment schedules

FPGA & Electrical Engineering Intern — May 2025 - August 2025

KLA Corporation, Broadband Plasma Wafer Inspection | Milpitas, CA

- Upgraded image compression FPGA firmware, achieving a 6.7% throughput increase on flagship inspection tools
- Architected Verilog pipelines for image segmentation and reconstruction, verifying functionality via Questa
- Deployed designs on Alveo accelerators, closing timing at 80MHz with 50% more parallel processing engines

Undergraduate Research Assistant — May 2024 - Present

IO Harness Project, CMU ECE | Pittsburgh, PA

- Developing a standardized research-chip harness to minimize infrastructure rework; testing a 180nm prototype
- Authored and validated SystemVerilog RTL for UART, I2C, and SPI communication blocks
- Streamlining a generation pipeline to produce custom eFPGAs serving as the device under test (DUT)

Power Electronics & Programming Intern — May 2023 - August 2023

Tau Motors, Stealth EV Startup | Redwood City, CA

- As first intern, spearheaded prototyping, layout, and validation of motor testbenches and PCBs
- Developed Python inventory management tools from scratch to accelerate hardware testing cycles

Leadership and Projects

Hybrid FFT/NTT Accelerator SoC — January 2026 - Present

- Designed a reconfigurable accelerator, executing an entire RTL-to-GDSII flow for tapeout in a 28nm node
- Integrated a RISC-V core in SpinalHDL to benchmark accelerator performance against software baselines
- Implemented a custom cocotb framework to verify the SoC across all design hierarchies and stages

Head Teaching Assistant (TA), Introduction to ECE (18-100) — January 2025 - January 2026

- Directed recruitment and managed a 40-TA team to inspire 180 students to pursue ECE as their field
- Redesigned labs to deliver engaging lessons, helping first-year students build a strong technical foundation
- Automated course admin via Python, empowering TAs to focus on teaching quality and student mentorship

Carnegie Involvement Association Buggy — August 2023 - Present

- Competed alongside a 50+ member team to build and race aerodynamic buggies, winning sweepstakes trophies
- Managed over $50k in club funds as treasurer, building dashboards to track ordering and financial workflows

Skills

- SystemVerilog/Verilog, SpinalHDL, cocotb, VCS/Questa/Xcelium, Quartus/Vivado, Cadence Physical Design Suite (Virtuoso/Genus/Innovus/Voltus/Conformal/SimVision), Cadence Allegro/KiCAD/Fusion360
- Python (NumPy, Pandas, Scikit-learn), C/C++, Lua, Bash, TCL, MATLAB, Git, Linux